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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,954	03/05/2002	Fumihiko Kato	FPM-02901	6433

26339 7590 03/09/2005

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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,954	KATO, FUMIHIKO	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 October 2004 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings were received on 18 May 2004 (Paper No. 5). These drawings are acceptable.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Due to the amendment filed on 14 October 2004, both independent claims 1 and 12 newly recite the limitation of "an impedance converter coupled to said output of said voltage selecting block." However, no support for this subject matter exists anywhere in the instant application. On the contrary, the specification teaches the voltage selecting block [Fig. 4; 34] operating as the final stage of the impedance converter [Fig. 4; 30] (see pages 11-13 of the specification).

6. Claims 2-7 and 13 are further rejected under 35 U.S.C. 112, first paragraph due to their dependency upon rejected base claims 1 and 12.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3-7, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Tamai et al. (US 6,160,533).

Regarding claim 1, Tamai discloses an LCD control unit for driving an LCD panel in an LCD device, the LCD control unit comprising: a signal controller [Fig. 1; 39] for generating a

voltage address signal [Fig. 4; LS] and a polarity control signal [Fig. 4; POLARITY INVERSION] (see Column 14, Line 27 - Column 15, Line 34); a voltage generator block [Fig. 4; 62] for generating a plurality of (n) γ-voltage levels [Fig. 4; at AS1-8] and a plurality of (m) Vcom-voltage levels [Fig. 1; Q], a voltage selecting block [Fig. 4; 63] for selecting a specified number of the γ-voltage levels and one of the Vcom-voltage levels based on the polarity control signal to output the specified number of γ-correction voltages and a Vcom voltage, wherein output of the voltage selecting block is selected from the plurality of (n) γ-voltage levels and the plurality of (m) Vcom-voltage levels according to a value of the voltage address signal; an impedance converter [Fig. 4; AS1-8], coupled to the output of the voltage selecting block to convert internal impedances of the γ-voltage levels and the Vcom-voltage levels and generate the specified number of the γ-correction voltages and the Vcom-voltage according to a value of the polarity signal; and an LCD driver [Fig. 1; 37] for generating a set of display data signals [Fig. 1; O1-ON] based on a set of external data signals [Fig. 1; D0-D2], wherein the LCD driver receives the specified number of the γ-correction voltages output from the voltage selecting block and includes a γ-correction section [Fig. 14; 37b] for correcting voltages of the display data signals based on the specified number of the γ-correction voltages (see Column 16, Line 14 - Column 17, Line 15 and Column 23, Lines 16-32).

Regarding claim 3, Tamai discloses the voltage generator block includes a resistor string [Fig. 4; 62] for generating n X L voltage levels, n first decoders [Fig. 14; DE1-DEN] for selecting [Fig. 14; ASW1-ASWN] the n γ-voltage levels [Fig. 14; 42a & 42b] from the n X L voltage levels based on the voltage address signal, and m second decoders [Fig. 15; DEi] for

selecting the m Vcom-voltage levels [Fig. 15; 42] from the n X L voltage levels based on the voltage address signal, given number L being an integer (see Column 23, Line 16 - Column 24, Line 35).

Regarding claim 4, Tamai discloses the specified number of γ-correction voltages are a pair of γ-correction voltages [Figs. 7 & 14; 42a & 42b] (see Column 18, Lines 40-46).

Regarding claim 5, Tamai discloses the voltage selecting block alternately selects the pair of γ-correction voltages having a positive polarity and the pair of γ-correction voltages having a negative polarity, with respect to the Vcom voltage (see Column 16, Lines 48-63).

Regarding claim 6, Tamai discloses the voltage generator block includes a resistor string [Fig. 4; 62] for generating a plurality of voltage levels, a decoder [Fig. 14; DE1-DEN] for decoding the voltage address signal, and a selector [Fig. 14; ASW1-ASWN] for selecting one of the γ-voltage levels or one of the Vcom voltage levels (see Column 23, Line 16 - Column 24, Line 35.

Regarding claim 7, Tamai discloses the LCD control unit is a one-chip IC (see Column 5, Lines 24-41).

Regarding claim 12, this claim is rejected by the reasoning applied in the above rejection of claim 1; furthermore Tamai discloses the voltage selecting block [Fig. 4; 63] being coupled to

the voltage generator block [Fig. 4; 62]; and wherein the display driver [Fig. 1; 37] receives the specified number of the γ-correction voltages [Fig. 4; at AS1-8] output from the impedance converter [Fig. 4; AS1-8] (see Column 16, Line 14 - Column 17, Line 15 and Column 23, Lines 16-32).

Regarding claim 13, Tamai discloses the γ-correction section [Fig. 14; 37b] generates a plurality of voltages based on the specified number of the γ-correction voltages [Fig. 4; at AS1-8], and the voltages of display data signals [Fig. 1; O1-ON] are selected from the plurality of voltages based on the set of external data signals [Fig. 1; D0-D2] (see Column 16, Line 14 - Column 17, Line 15 and Column 23, Lines 16-32).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamai et al. (US 6,160,533) in view of Gormish (US 5,910,796).

Regarding claim 2, Tamai does not expressly disclose the voltage address signal and the polarity control signal are generated based on a software as time series signals. However, Gormish discloses software controlling and setting gamma correction signals (see Column 1, Lines 12-46). Tamai and Gormish are analogous art because they are from the shared field of

gamma correcting display devices. Therefore, it would have been obvious to one skilled in the art to substitute Gormish's software control in the place of Tamai's hardware control, so as to provide a convenient means of gamma correcting the display for the user.

Response to Arguments

11. Applicant's arguments filed 14 October 2004 have been fully considered but they are not persuasive. The Applicant contends the cited prior art of Tamai et al. (US 6,160,533) neglects teaching generation of any output voltage according to a polarity signal and "instead, at best, the circuit 63 of Tamai generates an output signal based solely on the input signal thereto (i.e. the signals from the flip-flops FF1-FF8)" (see page 8 of the amendment). However, the examiner must respectfully disagree. Tamai's polarity signal [Fig. 4; POLARITY INVERSION] controls switches AS11-AS14, thereby affecting the voltage conversion transpiring and output at/by circuit elements AS1 and AS8 (see Column 16, Line 14 - Column 17, Line 15).

Additionally, the Applicant contends Tamai does not disclose an impedance converter. Again, the examiner respectfully disagrees. Tamai fully discloses a voltage selecting block [Fig. 4; 63] including an impedance converter [Fig. 4; AS1-8] that converts [i.e. transforms a signal level before the analog switch to a signal level after the analog switch] internal impedances of the γ-voltage levels [Fig. 4; voltages at AS1-8] and the Vcom-voltage levels [Fig. 1; Q] and generates the specified number of the γ-correction voltages and the Vcom-voltage (see Column 16, Line 14 - Column 17, Line 15 and Column 23, Lines 16-32), as currently claimed by Applicant. Note, the Applicant's argument of inventive novelty centers around the claimed operation of impedance level conversion. However, pending claims remain silent on the explicit

matter of what such levels are being converted to. As such, the examiner is relying on the broadest definition of "conversion" as would be understood by one skilled in the art.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.P.
4 March 2005

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